TWO DIMENSIONAL ADDRESSING OF A MATRIX-VECTOR REGISTER ARRAY

Abstract of the Disclosure

A processor and method for processing matrix data. The processor includes M independent vector register files which are adapted to collectively store a matrix of L data elements. Each data element has B binary bits. The matrix has N rows and M columns, and L=N*M. Each column has K subcolumns. $N \geq 2$, $M \geq 2$, $K \geq 1$, and $B \geq 1$. Each row and each subcolumn is addressable. The processor does not duplicatively store the L data elements. The matrix includes a set of arrays such that each array is a row or subcolumn of the matrix. The processor may execute an instruction that performs an operation on a first array of the set of arrays, such that the operation is performed with selectivity with respect to the data elements of the first array.